WHAT IS CLAIMED IS

1. A method of fabricating a semiconductor device, comprising the steps of:

forming an electronic circuit on a wafer in a region defined by a scribe line, said wafer carrying a first electrode thereon;

attaching a circuit substrate carrying thereon a predetermined conductor pattern, on said wafer, said circuit substrate carrying a second electrode and a third electrode, said step of attaching said circuit substrate including a step of aligning said circuit substrate with respect to said electronic circuit in said wafer;

interconnecting said first electrode on said wafer and second electrode of said predetermined conductor pattern by a wire bonding process;

forming a spherical electrode on said third electrode; and

dicing said wafer along said scribe line.

2. A method as claimed in claim 1, wherein said step of attaching including a step of bonding said circuit substrate to said wafer by an adhesive.

3. A method as claimed in claim 1, wherein said step of attaching said circuit substrate includes the steps of: placing said circuit substrate on said

wafer; aligning said circuit substrate with respect to said wafer; and lifting said circuit substrate in a direction generally perpendicular to said wafer by introducing a resin to a space between said wafer and said circuit substrate.

4. A method as claimed in claim 1, further comprising a step of encapsulating a bonding wire used in said wire bonding step and said first and second electrodes by a resin.

5. A method as claimed in claim 4, wherein said step of dicing along said scribe line is conducted along said resin.

6. A method as claimed in claim 1, further comprising a step of providing a resin along said scribe line, and wherein said step of dicing is conducted along said resin.

7. A method as claimed in claim 1, wherein said circuit substrate is formed of a polyimide tape carrying thereon a conductor pattern.

8. A method as claimed in claim 1, wherein said circuit substrate is formed of a glass epoxy carrying a conductor pattern.

9. A method as claimed in claim 1, wherein said wire bonding process is conducted first by bonding a first end of a bonding wire to said first electrode on said wafer and subsequently by bonding a second end of said bonding wire to said second electrode on said circuit substrate.

10. A method as claimed in claim 1, wherein said spherical electrode is formed by a solder bump.

11. A semiconductor device, comprising:

a semiconductor chip having a top surface, said semiconductor chip carrying a first electrode;

a circuit substrate attached to a top surface of said semiconductor chip, said circuit substrate carrying thereon a predetermined conductor pattern including a second electrode and a third electrode;

a resin layer intervening between said top surface of said semiconductor chip and said circuit substrate;

a spherical electrode provided on said circuit substrate in correspondence to said third electrode;

a bonding wire electrically interconnecting said second electrode of said predetermined conductor pattern on said circuit substrate and said first electrode on said semiconductor chip; and

a resin potting encapsulating said bonding wire including said first and second electrodes,

said chip and said resin potting being defined by a common edge surface substantially perpendicular to a principal surface of said substrate.

12. A semiconductor device as claimed in claim 11, wherein said resin layer is an adhesive layer.

13. A semiconductor device as claimed in claim 11, wherein said resin layer has a composition substantially identical with a composition of said resin potting.

14. A semiconductor device as claimed in claim 11, wherein said circuit substrate is formed of a glass epoxy.

15. A semiconductor device as claimed in

claim 11, wherein said circuit substrate is formed of a polyimide film.

16. A semiconductor device, comprising:

a semiconductor chip having a top surface, said semiconductor chip carrying a first electrode;

a circuit substrate attached to a top surface of said semiconductor chip, said circuit substrate carrying thereon a predetermined conductor pattern including a second electrode and a third electrode;

a spherical electrode provided on said circuit substrate in correspondence to said third electrode;

a bonding wire electrically interconnecting said second electrode of said predetermined conductor pattern on said circuit substrate and said first electrode on said semiconductor chip;

a resin potting encapsulating said bonding wire including said first and second electrodes;

a resin side wall cover covering a side wall of said circuit substrate;

said chip having a side wall substantially flush to an outer surface of said resin side wall cover, said side wall of said chip being substantially perpendicular to a principal surface of said chip.

17. A semiconductor device as claimed in claim 16, wherein said resin potting and said resin side wall cover have a substantially identical composition.